



☐ Tentative Specification
☒ Preliminary Specification
☐ Specification Approval

Specification For 4.2" EPD

Model Name: RSE0420N01

Version: V0

	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE			

CUSTOMER APPROVAL	SIGNATURE	DATE
	Notes:	

Notes :

- 1 、 Please contact before assigning your product based on this module specification.
- 2 、 To improve the quality of product, and this product specification is subject to change without any notice.

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1 General Description

SE042BG is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 4.2” active area contains 400x300 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic ShelfLabel (ESL) System.

2 Features

- ◆ 400×300 pixels display
- ◆ White reflectance above 30%
- ◆ Contrast ratio above 8:1
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape, portrait modes
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform stored in On-chip OTP
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor

3 Application

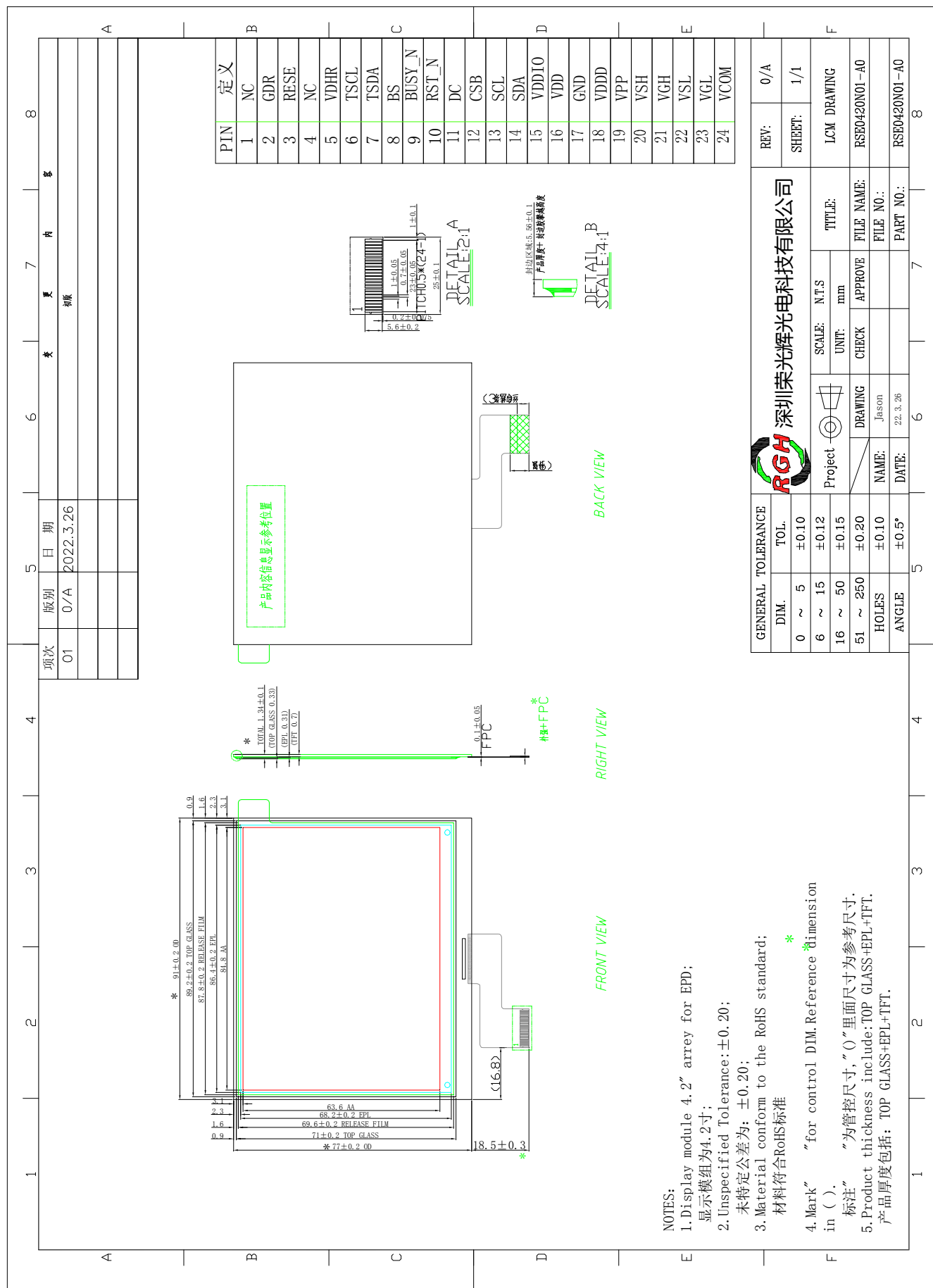
Electronic ShelfLabel System

4 Mechanical Specification

4.1 Dimension

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	120DPI
Active Area	84.80×63.60	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Square		
Outline Dimension	91(H)×77 (V) ×1.34(D)	mm	
Weight	18	g	

4.2 Mechanical Drawing of EPD Module



5 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSYN	O	Busy state output pin	Note 5-3
10	RSTN	I	Reset signal input. Active Low.	
11	D/C	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDD	P	Power Supply for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin Low when

- Outputting display waveform
 - Programming with OTP
 - Communicating with digital temperature sensor
- Note 5-4:

Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V _{dd}	-0.5 to +4.0	V
Logic Input voltage	V _{IN}	-0.5 to V _{dd} +0.5	V
Logic Output voltage	V _{OUT}	-0.5 to V _{dd} +0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operations should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V _{dd}	-	VDD	2.4	3.0	3.6	V
High level input voltage	V _{IH}	-	-	0.8 V _{dd}	-	-	V
Low level input voltage	V _{IL}	-	-	-	-	0.2 V _{dd}	V
High level output voltage	V _{OH}	IOH = -100uA	-	0.9 V _{dd}	-	-	V
Low level output voltage	V _{OL}	IOL = 100uA	-	-	-	0.1 V _{dd}	V
Typical power panel	P _{TYP}	-	-	-	45	240	mW
Deep sleep mode	P _{STPY}	-	-	-	3	-	uW
Typical operating current	Iopr_VDD	V _{dd} =3.0V	-	-	15	80	mA

Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	35	50	uA
Deep sleep mode current	IdslpVDD	VDD=3.0V DC/DC OFF No clock No output load Ram data not retain	VDD	-	1	-	uA
Operation temperature	T _{OPR}	-	-	0	-	50	°C
Operation relative humidity	RHop	-	-	-	-	70	%RH
Operation illuminance intensity	E	indoor only	-	-	-	2000	lux
Storage temperature	T _{STG}	-	-	-25	-	60	°C
Storage relative humidity	RHst	-	-	30	-	60	%RH

- Notes: 1. The typical power is measured with following transition from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 6-1)
2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by OED.

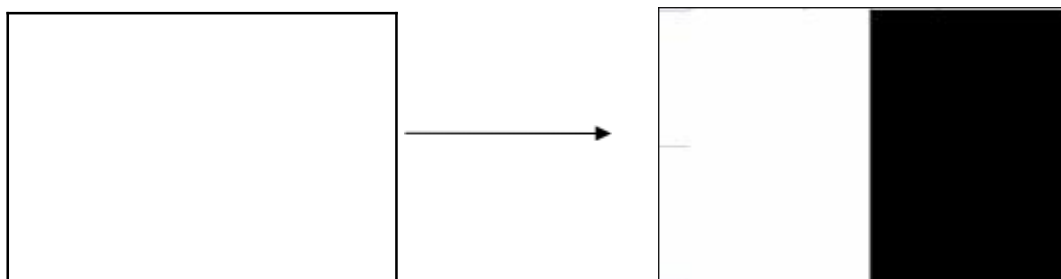


Figure 6-2 The typical power consumption measure pattern

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM		-1.5		V

6.4 MCU Interface

6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Connnand Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
4-wire SPI	SDIN	SCLK	CS#	D/C#	RES#
3-wire SPI	SDIN	SCLK	CS#	L	RES#

Table 6-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In 4-wire SPI mode, D0 actsas SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table 6-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C#is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

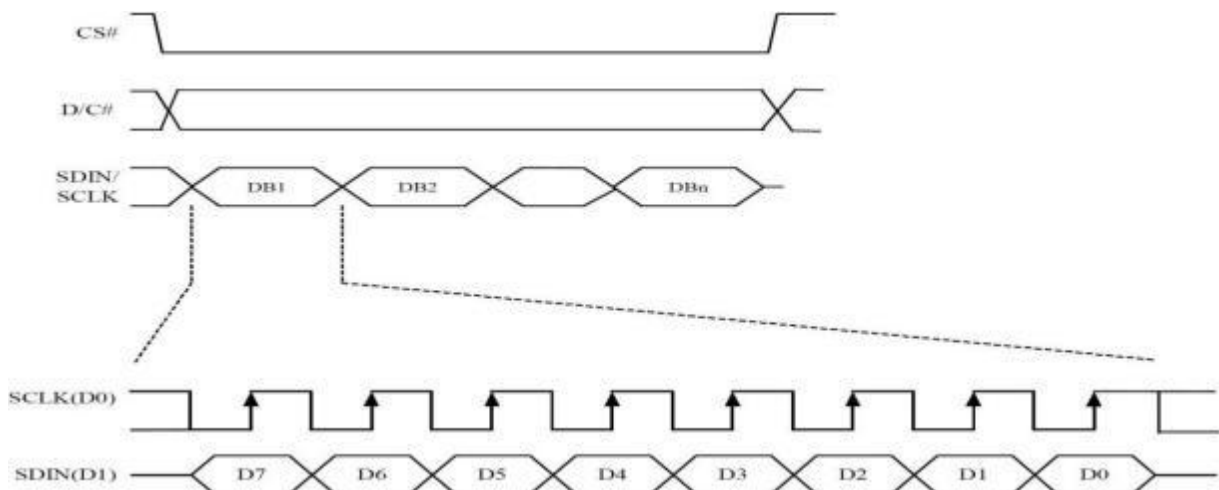


Figure 6-4-2: Write procedure in 4-wire SPI mode

6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Note: ↑ stands for rising edge of signal

Table 6-4-3: Control pins of 3-wire Serial interface

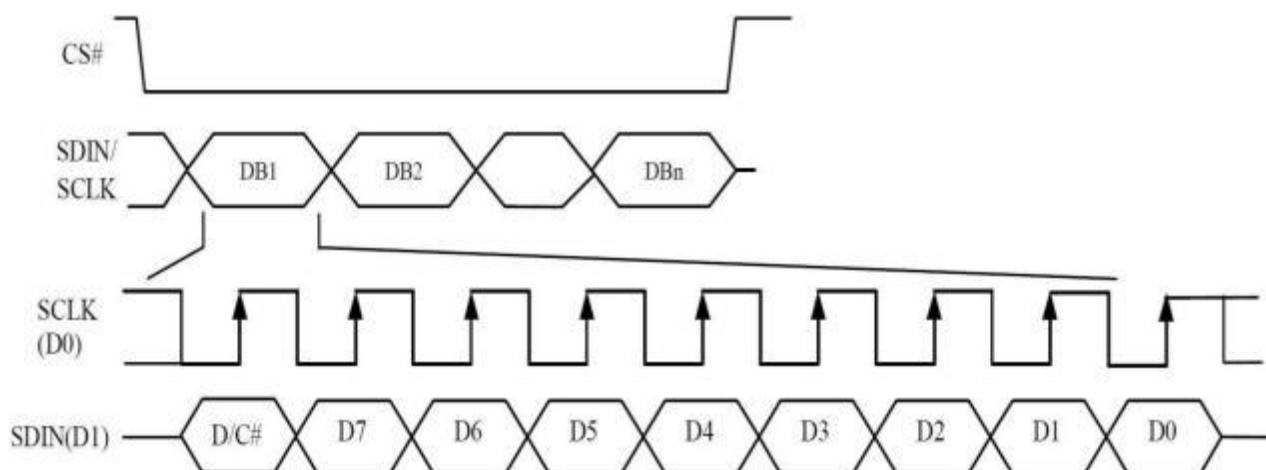


Figure 6-4-3: Write procedure in 3-wire SPI mode

7 Optical Specification

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	7- 1
CR	Contrast Ratio		8:1	10:1	-	-	7-2
White Δ L _{24h}	Reduce		-	≤ 4	-	-	-
T _{update}	Image update time	at 25 °C	-	2800	-	ms	-

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8 Handling, Safety, and Environment Requirements

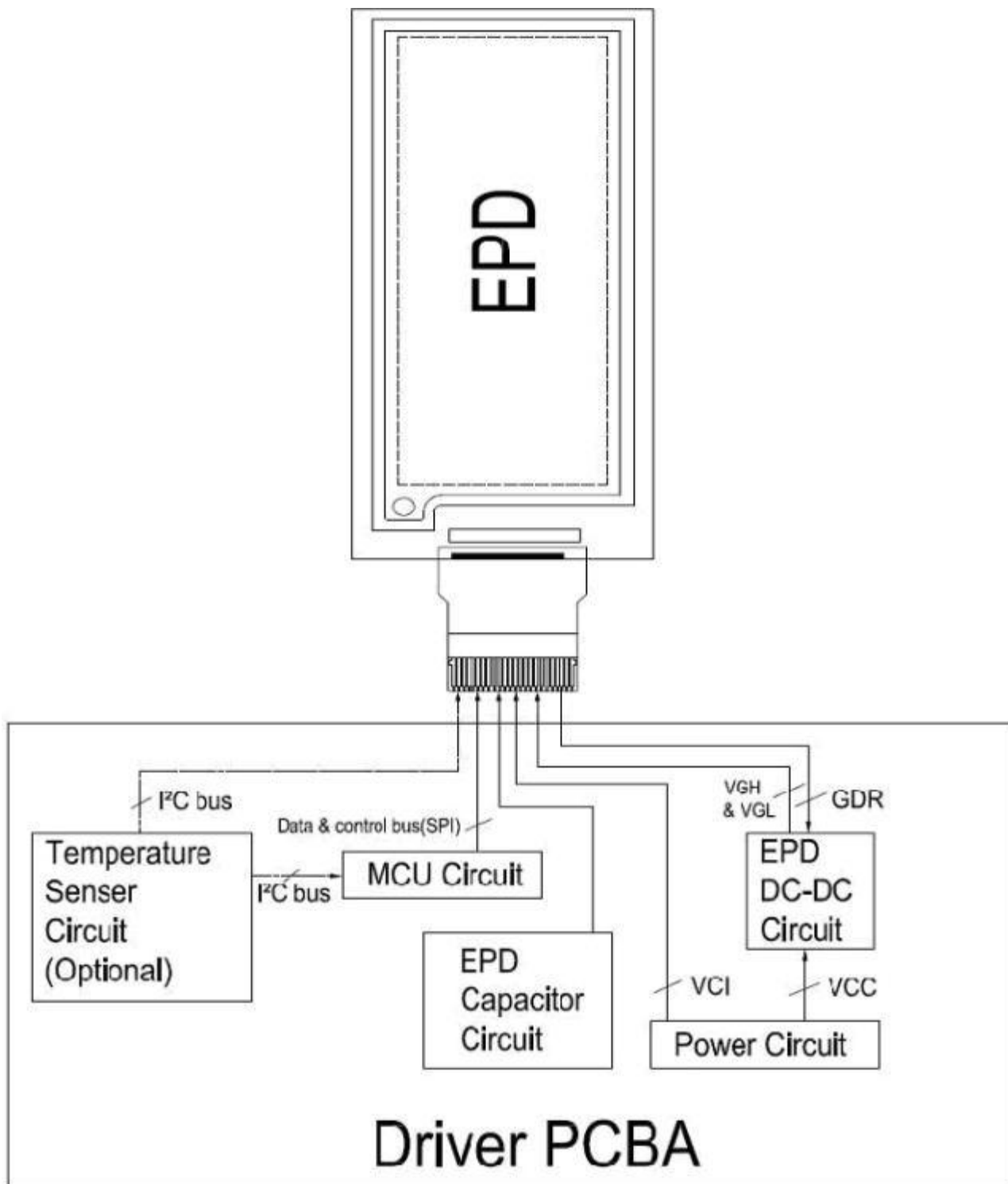
1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.

High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15°C to 35°C, and humidity from 30%RH to 60%RH.

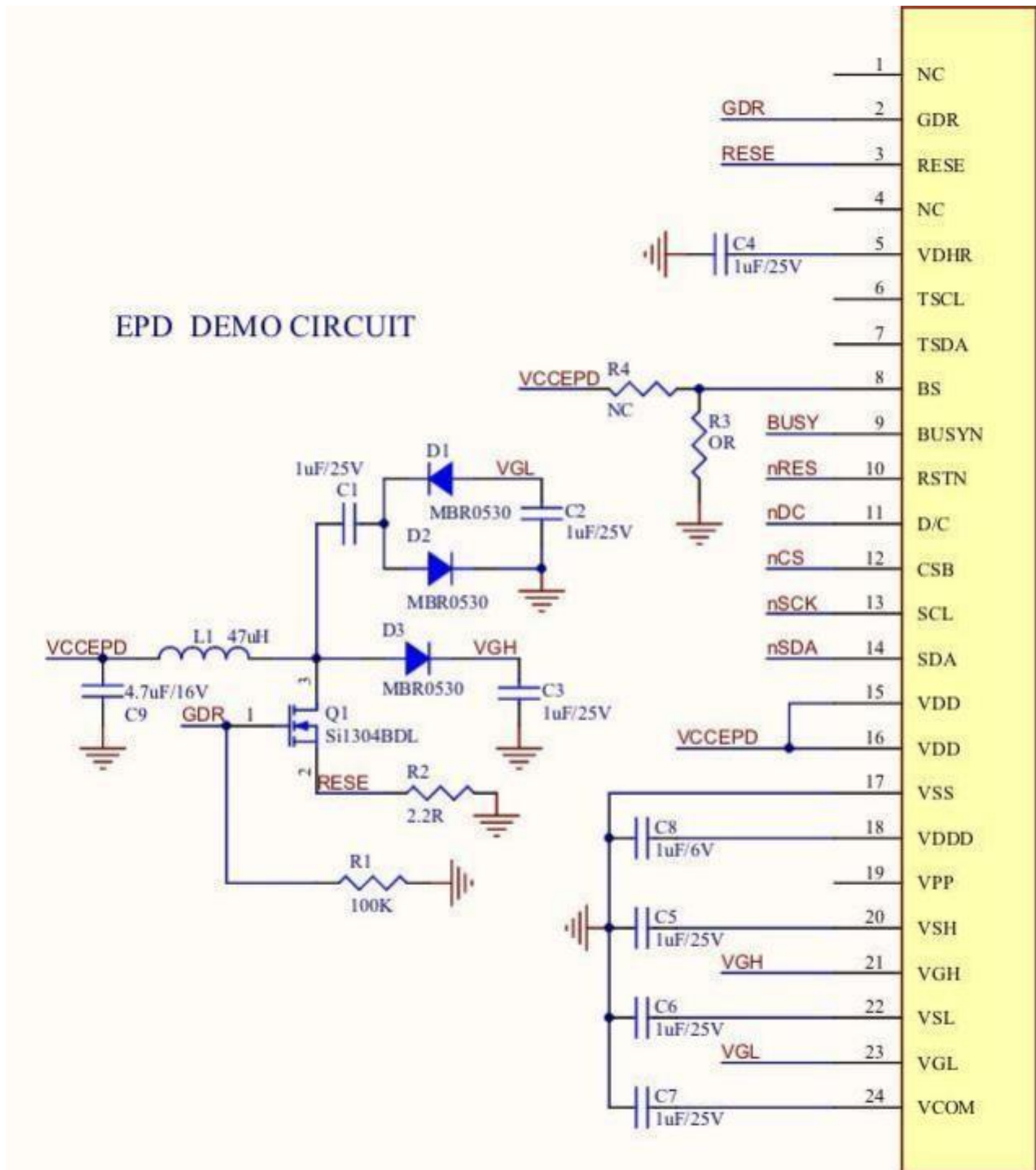
9 Reliability Test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

10 Block Diagram



11 Typical Application Circuit with SPI Interface



Notes: 11-1. The electronic elements should be tested and verified for Max Power. OED Recommend the above electronic elements.

12 Packaging

TBD

13 Mark and Bar Code Definition