深圳荣光辉光电科技有限公司

☐ Tentative Specification
☐ **Preliminary Specification**
☐ Specification Approval

Specification For 3.52” EPD

Model Name: RSE0352N01

Version: V0

	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE	Jungui Shen	Jacky Nong	James Wu
DATE	2021.9.24	2021.9.14	2021.9.14

	SIGNATURE	DATE
CUSTOMER APPROVAL		
	Notes:	

Notes：

1、Please contact before assigning your product based on this module specification.

2、To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
0.1	2021.6.10	First release	Preliminary
0.2	2021.7.19	Update Outline Dimension	P4,P5
0.3	2021.9.14	Update the drawing	P5
0.4	2021.9.24	Update Application Circuit	P14

CONTENTS

1. General Description

SE0352N01 is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white and black full display capabilities. The 3.52" active area contains 240x360 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- 240×360 pixels display
- White reflectance above 30%
- Contrast ratio above 8:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- Built-in temperature sensor

3. Application

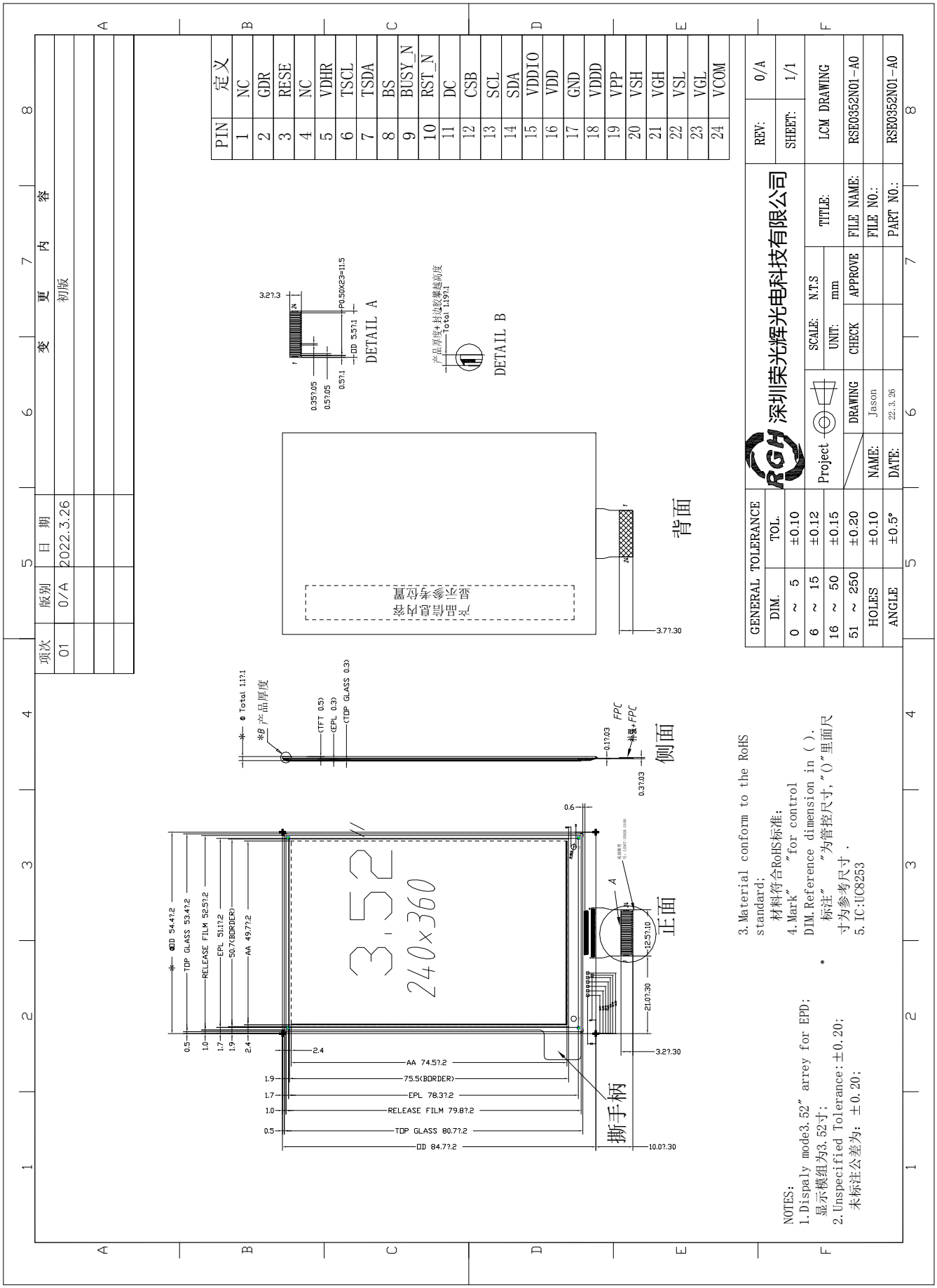
Electronic Shelf Label System

4. Mechanical Specification

4.1 Dimension

No.	Item	Contents	Unit
1	Screen Size	3.52 (Diagonal)	inch
2	Resolution(H*V)	240*360 Pixels	/
3	Pixel pitch (L*W)	TBD	mm
4	Interface type	SPI interface	/
5	Active area (L*W)	49 67*74 51	mm
6	Outline Dimension (L*W*H)	54.41*84.70*1.14	mm
7	Weight	TBD	G

4.2 Mechanical Drawing of EPD Module



5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	
5	VDHR	C	Positive source driver voltage for Source	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSY N	O	Busy state output pin	Note 5-3
10	RST N	I	Reset signal input. Active Low.	
11	DC	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins. It should be connected with VDD	
16	VDD	P	Power Supply for the chip	
17	GND	P	Ground	
18	VDDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.3 to V_{dd} +0.3	V
Logic Output voltage	V_{OUT}	-0.3 to V_{dd} +0.3	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{CI}	-	VDD	2.4	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{dd}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{dd}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{dd}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0 1 V_{dd}	V
Typical power panel	P_{TYP}	-	-	-	TBD	TBD	mW
Deep sleep mode	P_{STPY}	-	-	-	TBD	-	mW
Typical operating current	Iopr_VDD	V_{dd} =3.0V	-	-	TBD	TBD	mA

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	TBD	TBD	uA
Deep sleep mode current	Idslp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data not retain	VDD	-	TBD	TBD	uA
Operation temperature	T_{OPR}	-	-	0	-	50	℃
Operating relative humidity	RHop	-	-	-	-	70	%RH
Storage temperature	TSTG	-	-	-20	-	70	℃
Storage relative humidity	RHst	-	-	30	-	60	%RH

Notes: 1. The typical power is measured with following transition from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 6-1)

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by .

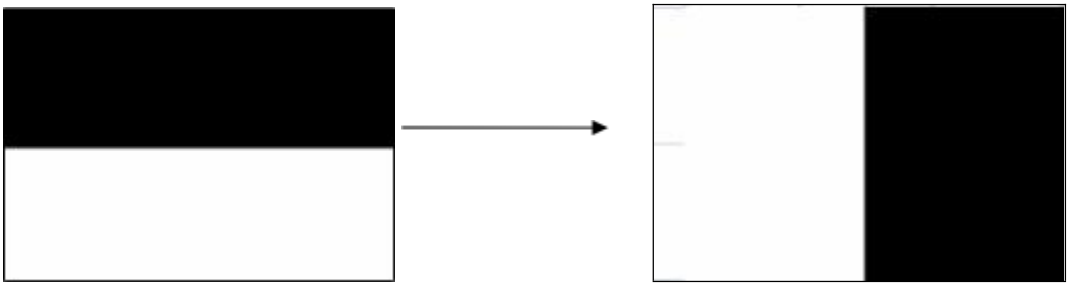


Figure 6-2 The typical power consumption measure pattern

6.3 Panel DC Characteristics (Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-4.0	-	-0.2	V
Positive Source output voltage	V_{SH}	-	S0-240	+14.5	+15	+15.5	V
Negative Source output voltage	V_{SL}	-	S0-240	-15.5	-15	-14.5	V
Positive gate output voltage	Vgh	-	G0-G360	+21	+22	+23	V
Negative gate output voltage	Vgl	-	G0-G360	-21	-20	-19	V

6.4 MCU Interface

6.4.1 MCU Interface Selection

The driver provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

Table 6-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

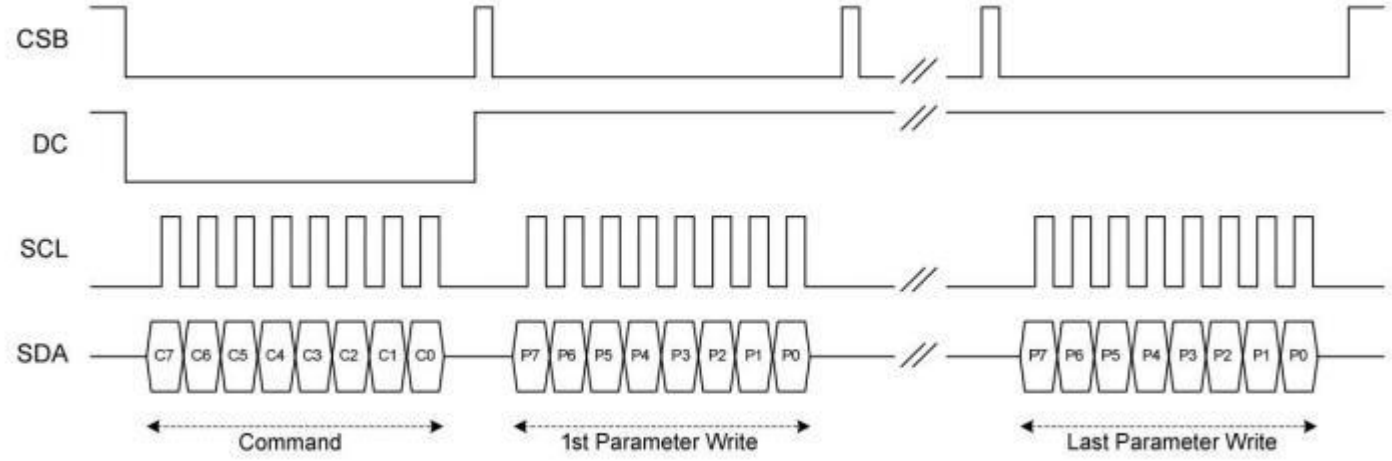


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

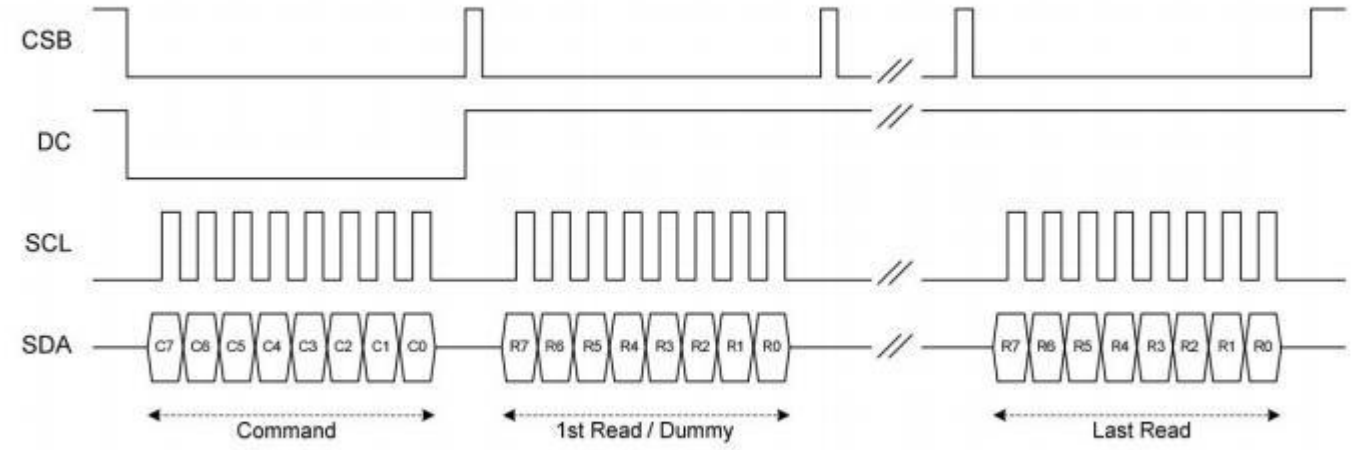


Figure: 4-wire SPI read operation

6.4.3 MCU Serial Interface (3-wire SPI)

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

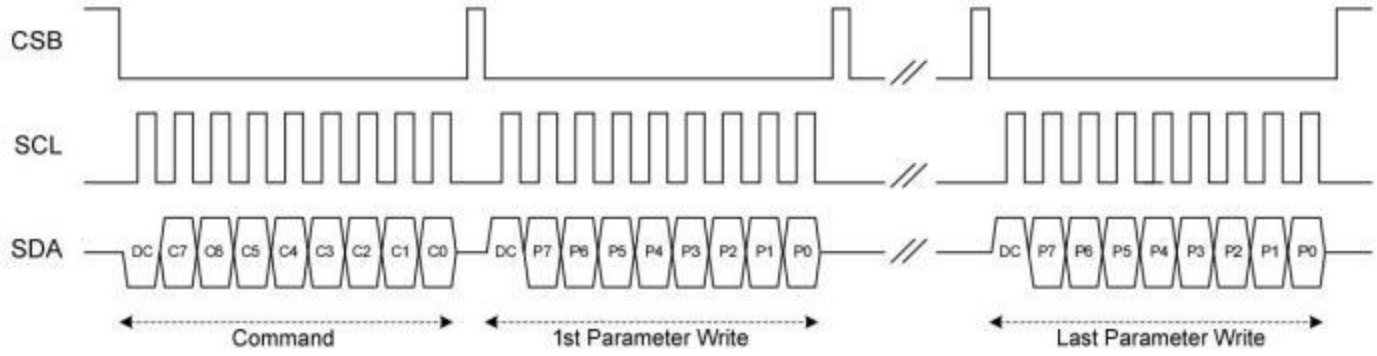


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

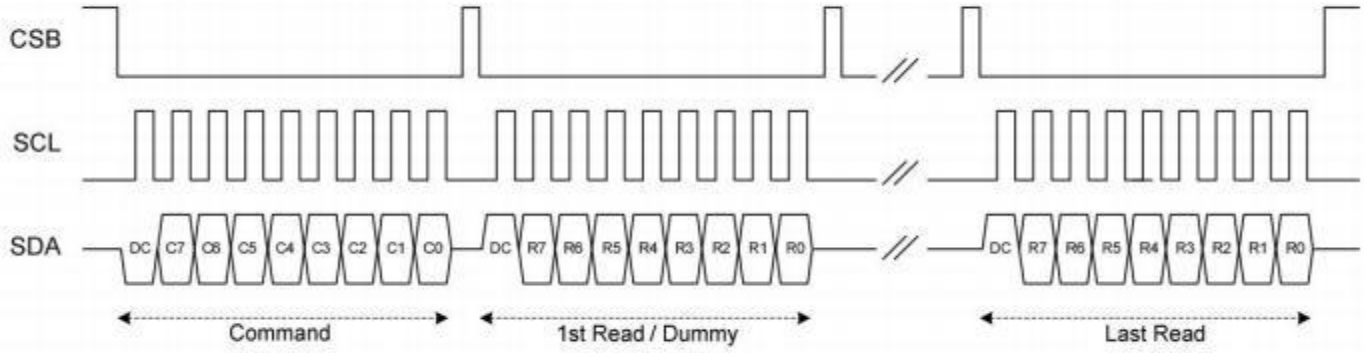


Figure: 3-wire SPI read operation

7. Optical Specification

Symbol	Parameter	Conditions	Values			Units	Notes
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	7-1
CR	Contrast Ratio		8:1	10:1	-	-	7-2
白△L 24h	Reduce		-	≤4	-	-	-
T_{update}	Image update time	at 25 °C	-	TBD	-	ms	-

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8. Handling, Safety, and Environment Requirements

Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

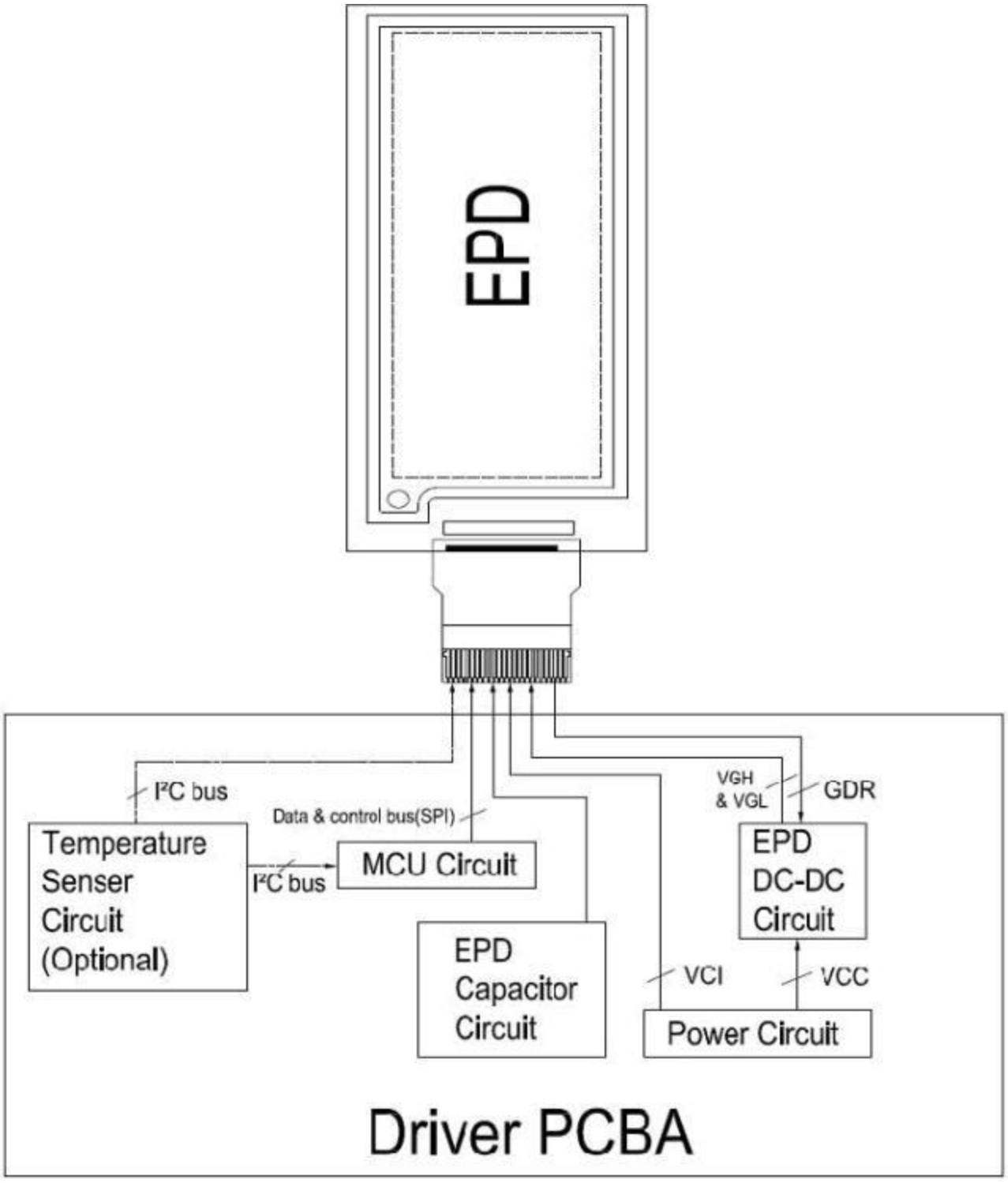
Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.
Disassembling the display module can cause permanent damage and invalidates the warranty agreements

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricality and other rough environmental conditions.

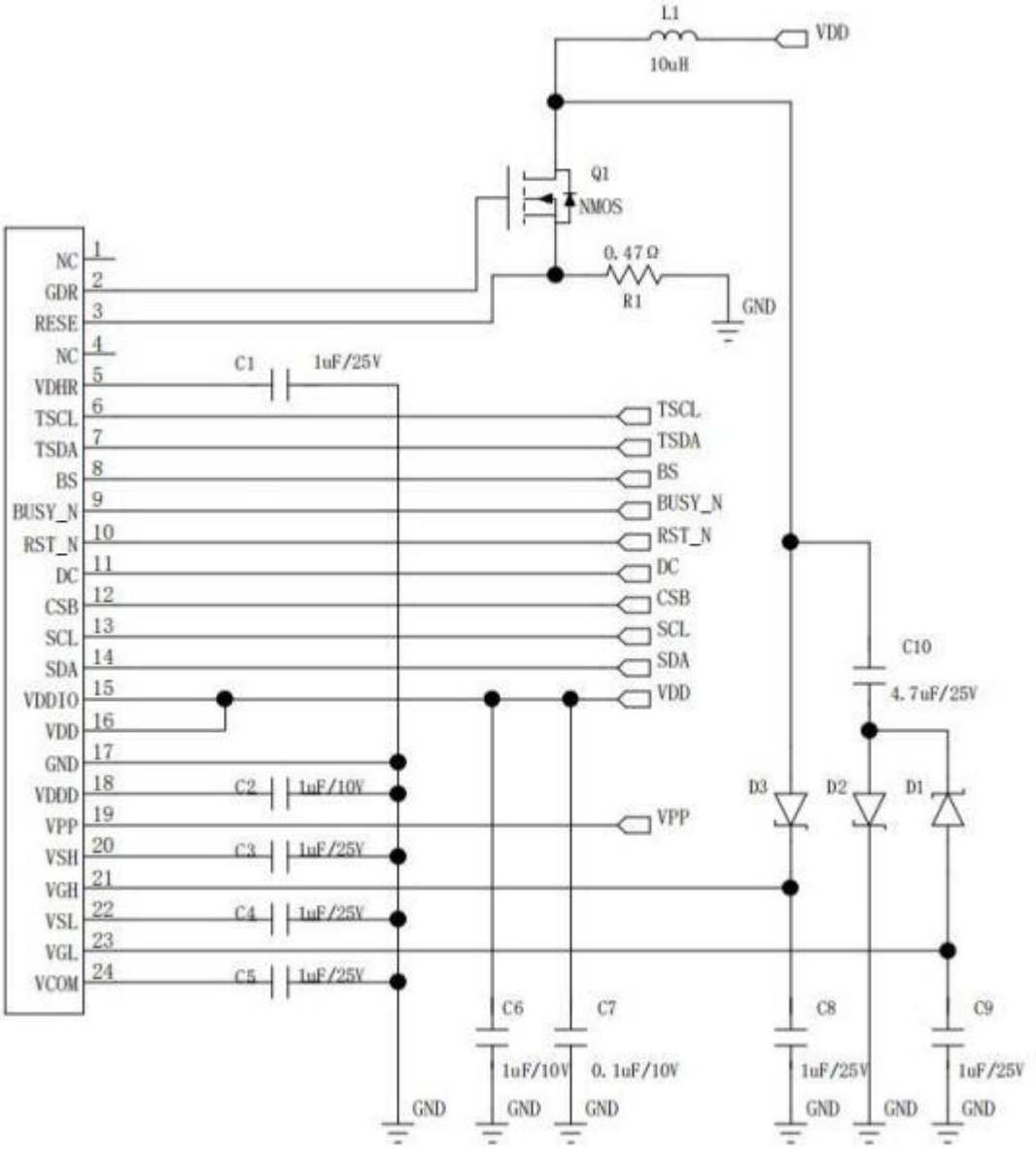
9. Reliability Test

No.	Test	Condition	Method	Remark
1	High Temperature Operation	T = +50°C, RH = 30% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low Temperature Operation	T = 0°C for 168 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
3	High Temperature Storage	T = +70°C, RH=23% for 168 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
4	Low Temperature Storage	T = -25°C for 168 hrs	IEC 60 068-2- 1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High Temperature, High Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature, High Humidity Storage	T = +60°C, RH=80% for 168hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70°C 30 min] : 50 cycles	IEC 60 068-2- 14	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each	Full packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179 IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

10. Block Diagram



11. Typical Application Circuit with SPI Interface



12. Packaging

TBD

13. Mark and Bar Code Definition

TBD